In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. Canceled

2. Canceled

3. Canceled

4. Canceled

5. Canceled

6. Canceled

7. Canceled

8. Canceled

9. Canceled

10. Canceled

11. (Previously presented) A memory cell, consisting essentially of:

a charge storage element;

a one-transistor switch constructed and arranged to selectively connect the storage element to a first data line, responsive to a first select signal; and

a one-transistor gain element having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line, responsive to a second select signal, the gain element comprising a FET having a first terminal connected to the storage element, a second terminal connected to the second data line and a third terminal selectively connected to one of a first power supply and a second power supply, the FET being symmetrical with respect to the second and third terminals.

12. (Previously presented) The memory cell of claim 11, wherein the FET is symmetrical with respect to the second and third terminals.

13. (Previously presented) The memory cell of claim 12, wherein the first terminal is a gate, the second terminal is a source and the third terminal is a drain.